identifying one of the phase shifted signals having a phase within a selected range of phases relative to the echo clock signal; and

generating the third set of data according to the identification of the phase shifted signal.

A4

19. The method of adjusting data timing according to claim 16 wherein the step of revising the initial output timing at the memory device includes the step of adjusting a vernier. –

REMARKS

Claims 1-19 are currently pending in the above-referenced patent application. Claims 1-15 have been presented for examination, and new claims 16-19 have been added. Claims 1-6, 8-11, and 13-15 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,577,236 to Johnson et al. ("Johnson"). Claim 7 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson and further in view of U.S. Patent No. 5,020,023 to Smith ("Smith"). Claim 12 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson and further in view of U.S. Patent No. 5,692,165 to Jeddeloh et al. ("Jeddeloh").

In response to the office action, applicant has amended claims 1, 6, 11, 12, and 14 in order to improve their form. Claims 16-19 have been added by this amendment.

Embodiments of the present invention are directed to a method of adjusting data timing and controlling data flow in a memory system by revising the relative phase relationship between clock signals of the memory controller and clock signals of a memory device. The revision of the phase relationship can be loosely described as follows. Assume that an initial output timing is established at the

memory device. The memory device transmits *to* the memory controller data (either read data or an echo clock signal) based on the initial output timing. The memory controller will then identify any phase error of the transmitted signal relative to a clock signal in the memory controller. Based on the identified phase error, the memory controller will transmit some control data that will be used by the memory device to *revise* the output timing that was initially established. Subsequent transmission of data from the memory device to the memory controller will be based on the *revised* output timing.

The Johnson patent discloses a memory system where the memory controller has a system clock circuit generating a system clock signal that is fed to the memory bank and (an inverted system clock signal) to the command driver. The command driver sends read commands to the memory bank according to the system clock signal. See col. 5, line 47-col. 6, line 18.

The memory controller described in the Johnson Patent also has a sampling clock circuit providing multiple sampling clock signals, each having a phase shift relative to the system clock signal. A multiplexer selects one of the sampling clock signals to be fed into a delay module, the output of which is fed to a first receiver that synchronizes a latch to accept read data transmitted by the memory bank. See col. 6, lines 8-46. The delay module preferably includes an off-chip supplementary delay unit of a fixed value. The delay value can be adjusted only by physically replacing the off-chip delay unit with one having the desired delay value. See col. 6, line 53-col. 7, line 20.

Selection of which sampling clock signal to feed to the delay module is based on information fed to the multiplexer from the data source. The information coming from the data source may be provided by either "automatic" or "manual" means. See col. 8, line 33-col. 9, line 3. However, once the information in the data source is established, the multiplexer cannot select any other sampling clock signal

until the information in the data source is either reprogrammed or manually changed. See col. 8, lines 41-44, and col. 8, lines 60-64.

The Johnson patent does not disclose a structure or operation where the memory controller identifies a phase error between a signal transmitted from the memory device and a clock signal of the memory controller, and then transmits data to the memory device in order to revise output timing according to the identified phase error. The structure disclosed by the Johnson patent is designed such that the memory bank transmits only read data to the memory controller; there are no clock signals transmitted by the memory bank to the memory controller as with embodiments of the present invention. Furthermore, the selection of the sampling clock signal in the Johnson system cannot be changed without physically changing switches or reprogramming a flash memory. Although the structure disclosed in the Johnson patent does include a delay module, the delay value is fixed and cannot be modified without replacing the off chip delay unit with a desired delay value.

Claims 1 and 6 are clearly not anticipated by the Johnson Patent. Claim 1 specifies a method of adjusting data timing in which the output timing at the memory device is initially determined and is then subsequently revised. The output timing is revised by first "transmitting an echo clock signal from the memory device to the memory controller according to the initial output timing." After the echo clock signal is received at the memory controller, the memory controller identifies "a phase error of the received echo clock signal relative to the master clock signal" and "transmits control data to the memory device for revising the initial output timing in response to the identified phase error to produce a revised output timing." Thereafter, the memory device revises the initial output timing to transmit a second set of data to the memory controller according to the revised output timing.

As explained above, the system disclosed in the Johnson Patent does not include a memory device that transmits an echo clock signal to a memory controller according to an initial output timing, as recited in claim 1. Instead, as explained

above, the Johnson memory device transmits only read data to the memory controller. Furthermore, the Johnson patent does not disclose a memory controller that identifies a phase error between a received echo clock signal relative to a master clock signal, as further recited claim 1. Nor does the Johnson system transmit data to the memory device to revise the initial output timing in response to the identified phase error, as also recited in claim 1.

Claims 6 is also not anticipated by the Johnson Patent because it specifies that the memory device produces an echo signal in response to a first read command, and transmits the echo signal to the memory controller. As explained above, Johnson's memory device transmits only data to the memory controller; it does not transmit a clock or echo signal to the memory controller. Claim 6 further specifies that the memory controller compares the received echo signal to a master clock signal and uses that comparison to select an adjusted time delay. The memory device then responds to a second read command by transmitting a second set of data to the memory controller with the adjusted time delay. As further explained above, the Johnson system does not include any circuitry for performing these functions.

Thus, for the foregoing reasons, claims 1 and 6 are patentably distinguishable from the Johnson patent. Claims 2-5 and claims 8-9, which depend from claims 1 and 6, respectively, are similarly allowable for the reasons set forth above. Therefore, the rejection of claims 1-6 and 8-9 under 35 U.S.C. § 102(e) should be withdrawn.

Claims 10-11, and 13-15 have been rejected under 35 U.S.C. § 102(e) as being anticipated by the Johnson reference.

Claim 10 is directed to a memory controller for a memory system containing memory devices that produce echo signals in response to master clock signals applied to a clock bus from a master clock source in the memory controller. The memory controller includes a phase comparing circuit that produces a phase signal in response to a phase difference between the echo signal and the master clock

signal. The claim further specifies that the memory controller includes a logic circuit that produces adjustment data in response to the phase signal, and a control data circuit adapted to produce a command signal in response to the adjustment data.

Claim 13, which the Examiner considers to be anticipated by the Johnson patent, is directed to a memory system, including a memory controller and a memory device interconnected by various buses. The memory device is specified as having an echo signal generator that generates an echo signal in response to a master clock signal. The memory device further includes a data latch that transmits data to a data bus responsive to a control signal applied to trigger input of the latch. Finally, the memory device includes a variable delay circuit that responds to an adjust command on a command bus to produce the control signal at a time corresponding to the adjust command. Claim 13 further specifies that the memory controller includes a phase comparator that produces an adjust command responsive to a phase difference between a master clock signal from a master clock generator and an echo signal from the echo signal generator.

The Johnson system does not anticipate the subject matter of claims 10 and 13. More specifically, the Johnson system does not have a phase comparing circuit which compares the phase difference between a signal transmitted by the memory device and a clock signal of the memory controller. The system shown in Figure 3 and described in col. 5, line 19-col. 7, line 40 does not include a phase comparing circuit that compares the phase error between a clock signal transmitted from the memory bank to the memory controller or a logic circuit that produces a signal in response to the output of the phase comparing circuit. What is shown and described is a system where a clock signal is selected by providing to a multiplexer predetermined information encoded in a hardware data source. None of the clock signals can be modified (*i.e.*, the relative phase relationship of the output of the sampling clock is fixed) nor can the selection of which clock signal to transmit to the delay module be changed unless the predetermined information from the hardware

data source is reprogrammed or manually switched. Furthermore, additional delay of the selected clock signal is possible only by inserting a fixed, off-chip delay unit into the signal path; the delay value can only be modified by replacing that fixed delay unit with another fixed delay unit having a different delay value.

For the foregoing reasons, claims 10 and 13 are not anticipated by the Johnson patent. Claims 11 and 14-15, which depend from claims 10 and 13, respectively, are similarly allowable for the reasons set forth above. Therefore, the rejection of claims 10-11, and 13-15 under 35 U.S.C. § 102(e) should be withdrawn.

Claim 7 has been rejected under 35 U.S.C. 103(a) as being obvious over Johnson, in view of Smith. Claim 7, which is dependent on claim 6, adds the limitation of adjusting a vernier to select the adjusted time delay. After the memory device transmits an echo clock signal to the memory controller, the echo clock signal and the master clock signal are compared to determine their relative phase difference. Adjustment of the vernier is made based on the relative phase error determined from the comparison.

The Smith patent discloses a system using a FIFO buffer and a technique of marking "frames" of a data stream to remove skew between multiple correlated synchronous data streams. See col. 5, line 40-col. 7, line 15. Data is placed into a FIFO register with the frame encoding and then removed from the FIFO buffer when the data is to be consumed. If a synchronization fault is detected when the data is unloaded from the FIFO buffer, a re-synchronization procedure is triggered. The procedure described in the Smith patent entails: inhibiting the unloading and loading of the FIFO buffer, purging the FIFO buffer, reloading data into the FIFO buffer while monitoring for the next frame mark, and when the next frame mark is detected, re-enabling normal loading and unloading of the FIFO buffer where unloading starts with the frame marked data. See col. 6, line 60-col. 7, line 15, and Figure 5.

The deficiencies of the Johnson reference, as discussed above, are not made up for by the Smith patent. The Smith patent uses the term "Vernier

Synchronization" and "Vernier Skew compensation" to simply describe the fact that frame synchronization used by the disclosed system may be made by adjusting in increments of *fractional* frame skew, as compared to *whole* frame synchronization. See col. 7, lines 16-21. Smith's use of "vernier" has nothing to do with disclosing or suggesting adjusting a vernier in adjusting a time delay in response to the relative phase relationship between two signals. Smith's reference to "vernier" simply describes making adjustments in less than whole increments.

Therefore, claim 7 is patentable over Johnson in view of Smith so that the rejection of claim 7 under 35 U.S.C. § 103(a) should be withdrawn.

Claim 12 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson, in view of Jeddeloh. Claim 12, which is dependent of claims 10 and 11, describes the memory controller as having a signal source that includes a multiple delay-locked loop. As referenced by the Examiner, the Jeddeloh reference describes the use of *phase* locked loops (not a *delay*-locked loop) in the prior art as an ineffective means of resolving problems associated with signal skew in high speed data processing environments. See col. 1, lines 31-45, in BACKGROUND OF THE INVENTION. The system disclosed in the Jeddeloh patent is designed to overcome the deficiencies by realigning a skewed clock signal to a second clock signal by adding an overall alignment delay equal to the sum of the propagation delays of the skewed clock signal. See col. 5, line 61-col. 6, line 4.

The deficiencies of the Johnson patent, as discussed above, are not made up for by the Jeddeloh reference. The Jeddeloh reference mentions the use of *phase* locked loops. In contrast, applicant claims a *delay*-locked loop in the signal source in order to produce a plurality of phase-shifted signals. Jeddeloh fails to mention a delay-locked loop at all. It follows then that the prior art reference does not suggest or provide the motivation to combine the elements recited in claim 12. Therefore, claim 12 is patentable over the Johnson patent in view of the Jeddeloh patent, and the rejection of claim 12 under 35 U.S.C. § 103(a) should be withdrawn.

New claims 16-19 have been added by this amendment. No new matter has been added. It is respectfully submitted that claims 16-19 are in condition for allowance.

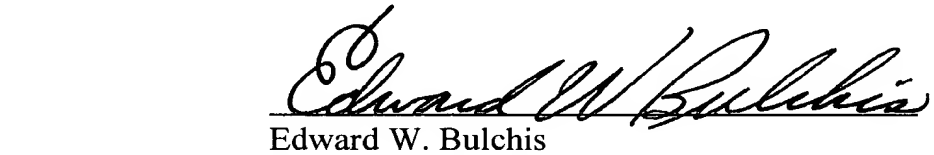
In view of the foregoing, it is respectfully submitted that the above-captioned patent application and all of the claims are in condition for allowance. If the Examiner has any questions regarding this matter, applicant request the Examiner contact the undersigned at the number listed below for a telephonic interview.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

Brent Keeth

SEED and BERRY LLP



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